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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/700,790

11/03/2003

Ernest Allen III

03-0722/LSIIP231

5485

7590

02/17/2005

LSI Logic Corporation  
1551 McCarthy Boulevard  
Milpitas, CA 95035

EXAMINER

NGHIEM, MICHAEL P

ART UNIT

PAPER NUMBER

2863

DATE MAILED: 02/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

10/700,790

Applicant(s)

ALLEN ET AL.

Examiner

Michael P. Nghiem

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1 and 3-13 is/are allowed.
- 6) ☒ Claim(s) 18-20 is/are rejected.
- 7) ☒ Claim(s) 2 and 14-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Specification***

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o).

Correction of the following is required:

Claim 1, "applying a second reference voltage having a value different from the first reference voltage to the first input of the first monitor cell" is not described in the specification.

Claim 3, "applying sequentially the first reference voltage and the second reference voltage to a first input of a second of the at least one monitor cells" is not described in the specification.

Claim 3, "applying a second test voltage from a second selected portion of the chip to a second input of the second monitor cell" is not described in the specification.

### ***Claim Objections***

2. Claims 2, 14, 18, and 20 are objected to because of the following informalities:

- claim 2, "e)" (line 3) should be – f) --.

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- claim 14, "a first and second latch" (line 10) should be -- a first latch and a second latch --.

- claim 18, The "integrated circuit" (line 1) cannot comprise itself (line 3).

- claim 20, "the latches" (line 3) lack antecedent basis.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa (US 4,713,819).

Regarding claim 18, Yoshikawa discloses an integrated circuit adapted for voltage level detection (Fig. 2), the integrated circuit comprising:

- an integrated circuit (6) having a plurality of voltage supply conductors (conductors from 631, 632) configured for providing a power supply voltage (output of 62) to the integrated circuit (Fig. 2);

- a monitor cell (comprises 63a, 63b) integrated in the integrated circuit for testing over and under voltage conditions (column 4, lines 6-14), the monitor circuit comprising two digital voltage comparators (63a, 63b) each of the comparators coupled respectively to a latch (65) for receiving the output of the voltage comparator (Fig. 2), wherein an input of each of the comparators is coupled to one of the plurality of voltage supply conductors (Fig. 2).

Regarding claim 19, Yoshikawa discloses that the monitor cell is further configured to receive at an input of each comparator a reference voltage (631, 632) provided by one of the plurality of voltage supply conductors for comparison with the supply voltage (Fig. 2).

Regarding claim 20, Yoshikawa discloses that the monitor cell is configured to receive a reference voltage (631, 632) from automated test equipment (comprises 3-5, Fig. 1) and to transmit outputs (61) of the latch to the automated test equipment (Fig. 2).

### ***Allowable Subject Matter***

4. Claim 2 would be allowable if rewritten to overcome the objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

5. Claim 14-17 would be allowable if rewritten or amended to overcome the objection set forth in this Office action.

6. Claims 1 and 3-13 are allowed.

### ***Reasons For Allowance***

7. The method as claimed wherein applying a second reference voltage having a value different from the first reference voltage to the first input of the first monitor cell (claim 1) or storing the first and second determinations in a first latch and a second latch attached respectively to the first and second comparators (claim 14) is not disclosed, suggested, or made obvious by the prior art of record.

### ***Contact Information***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael P Nghiem whose telephone number is (571) 272-2277. The examiner can normally be reached on M-H.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**MICHAEL NGHIEM**  
**PRIMARY EXAMINER**

Michael Nghiem

February 15, 2005